On the Limits of Noise Performance of Field Effect Transistors

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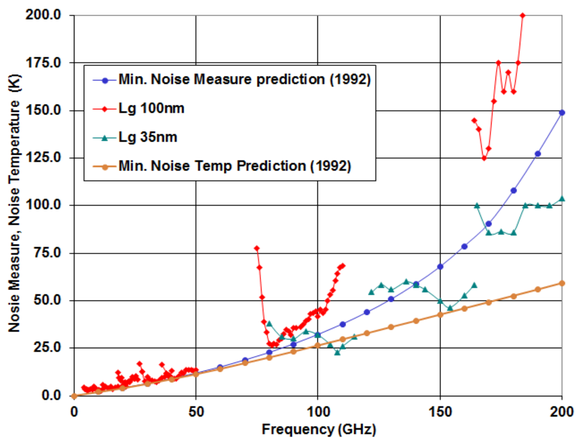
STATUS QUO

Noise Temperature of Cryogenic Amplifiers
State-of–the-Art 2016



NEW INSIGHTS

Device Scaling: Gate Length

$$T_{min} \cong 2\frac{f}{f_t}\sqrt{g_{ds}\,T_d\,r_t\,T_g} \cong \frac{f}{f_{max}}\sqrt{T_d T_a}$$

$L_g \searrow$ $f_{max} \nearrow$ $T_{min} \searrow$ if $T_d \approx const.$

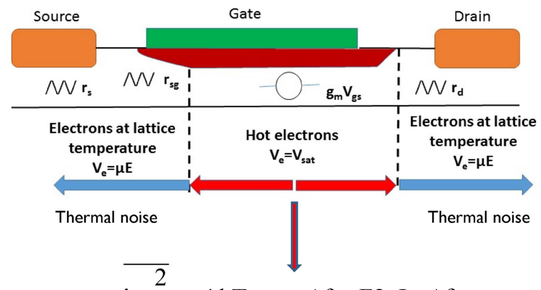
But within a measurement error no device demonstrated T_{min} lower than that predicted 25 years ago.

The best cryogenic wafers: Chalmers (130 nm), NGSTCryo3 (80-100 nm), NGST (35 nm) exhibit progressively better f_{max} and M_{min} but about the same minimum T_{min} because T_d increases for deep submicron gate lengths.

Why?

DESCRIPTION

General and (Very Simple) Picture of Noise in FETs:

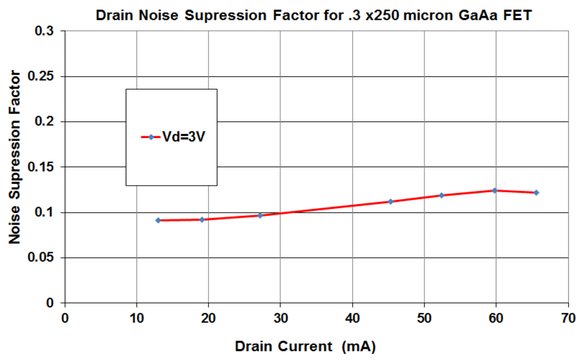


$$\overline{i_{ds}^{\,2}} = 4kT_d\,g_{ds}\,\Delta f = F2qI_d\,\Delta f$$

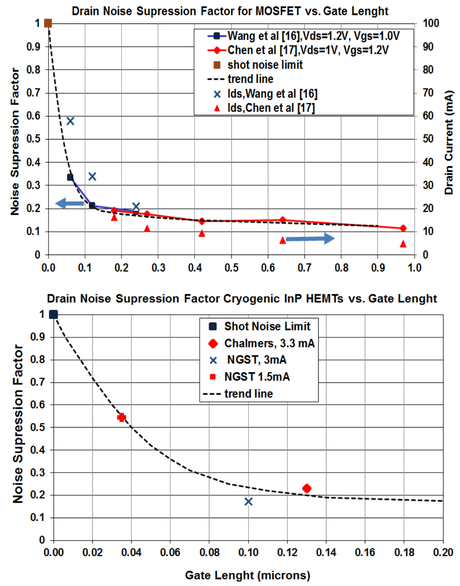
F shot noise suppression factor

F should:

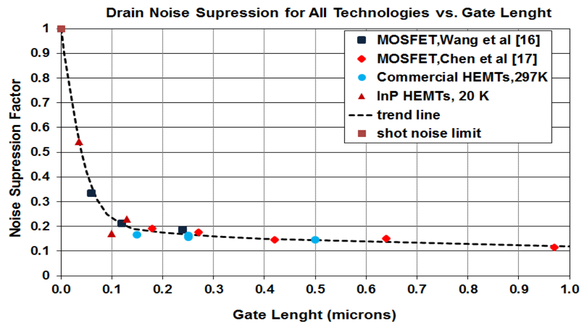
- be approximately independent of FET bias and its physical temperature.
- for long gates F should assume a constant value while for short gates it should increase as in the limit for $L_g \to 0$, a pure shot noise should be observed and $F \to 1$.
- As the average energies of hot electrons in Si, GaAs and InGaAs which form channels of all modern FETs are not that different for electric fields larger than 10^4 V/cm (1 eV), Γ^2 should be only weakly dependent on a particular semiconductor structure



QUANTITATIVE IMPACT



PROPOSED CONCEPT GOALS



It should be possible to produce plots of F= $f(L_g)$ for any foundry process which, in turn, would allow for the computation of noise parameters at any bias and at any temperature, given the known equivalent circuit.